Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing Of Claims:

Claims 1-10. (Canceled).

11. (Currently Amended) A device for forming a signature, comprising:

a ~~predefined number of~~ shift register ~~registers~~ having a predefined number of bit position memory devices ~~positions~~, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices ~~shift registers~~ after a predefined number of applied data words and cycles; and

a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature.

12. (Currently Amended) The device according to claim 11, wherein the individual ~~shift registers~~ bit position memory devices are connected by antivalence points, and the individual bits of the data words at the antivalence points, as well as the at least one additional bit position of the code generator, are inserted to form the signature.

13. (Currently Amended) The device according to claim 11, wherein the individual ~~shift registers~~ bit position memory devices are connected by equivalence points, and the individual bits of the data words, as well as the at least one additional bit position of the code generator, are inserted at the equivalence points to form the signature.

14. (Currently Amended) The device according to claim 11, wherein the code generator implements an ECC code and inputs a number of bit positions corresponding to the ECC code being used into a corresponding number of additional ~~shift registers~~ bit position memory devices to form the signature.

15. (Currently Amended) The device according to claim 11, wherein the code generator forms a parity bit and inputs it in an additional bit position memory device of the shift register.

16. (Previously Presented) The device according to claim 14, wherein the code generator implements a Hamming code.

17. (Previously Presented) The device according to claim 14, wherein the code generator implements a Berger code.

18. (Previously Presented) The device according to claim 14, wherein the code generator implements a Bose-Lin code.

19. (Previously Presented) The device according to claim 14, wherein the code generator implements a generic code generator table.

20. (Currently Amended) A method for forming a signature, comprising:

providing a ~~predefined number of~~ shift register ~~registers~~ having a predefined number of bit position memory devices ~~positions~~, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices ~~shift registers~~ after a predefined number of applied data words and cycles; and

providing a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature.